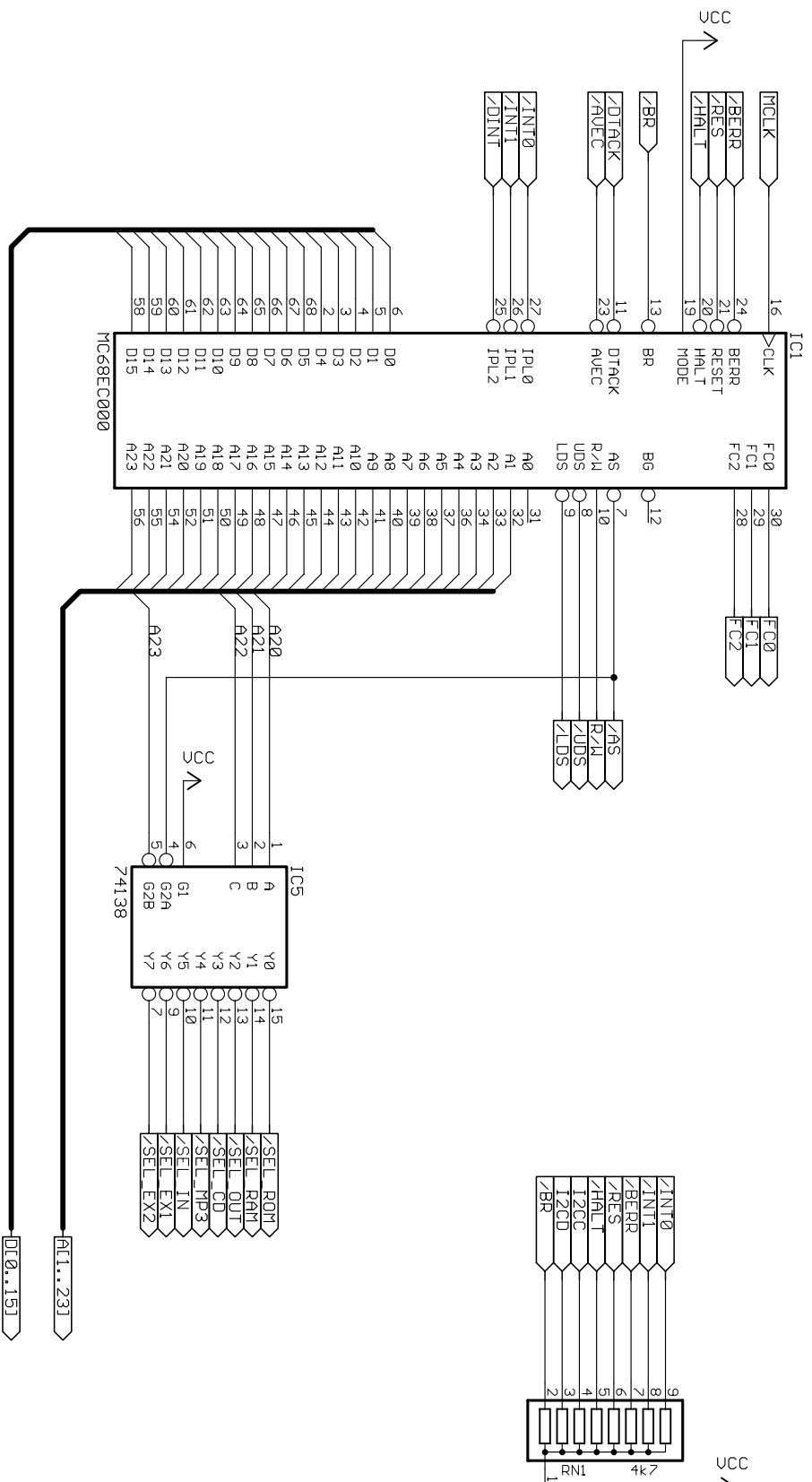


CPU



CPU

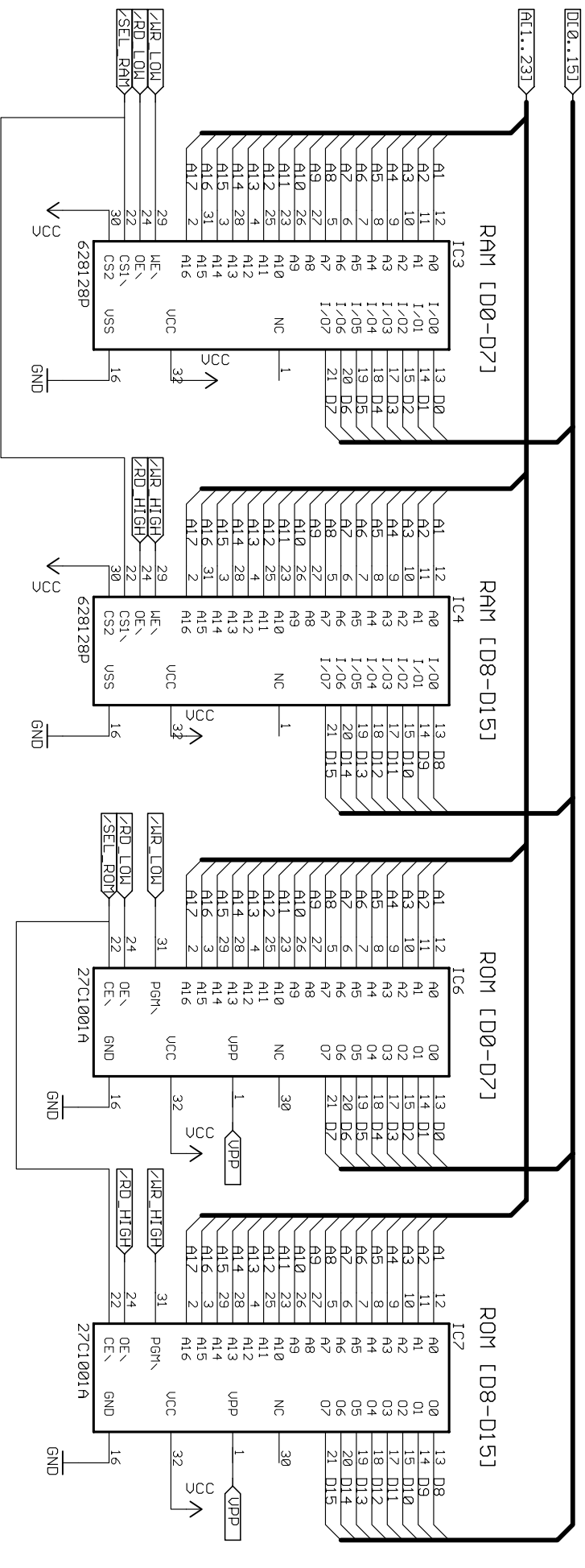
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REV: 003

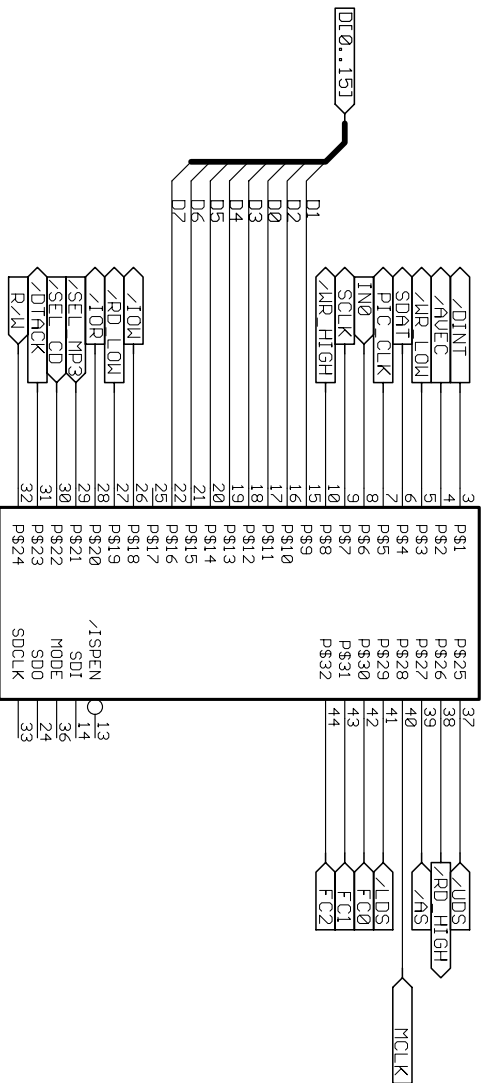
Date: 17. 04. 2000 08:57:00

Sheet: 1/1

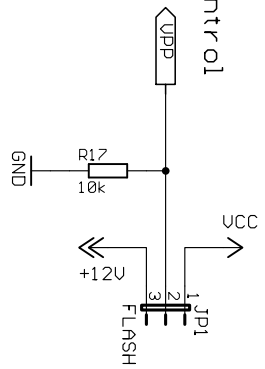


Addr. Decoder

US146



Write Control



RAM, ROM . . .

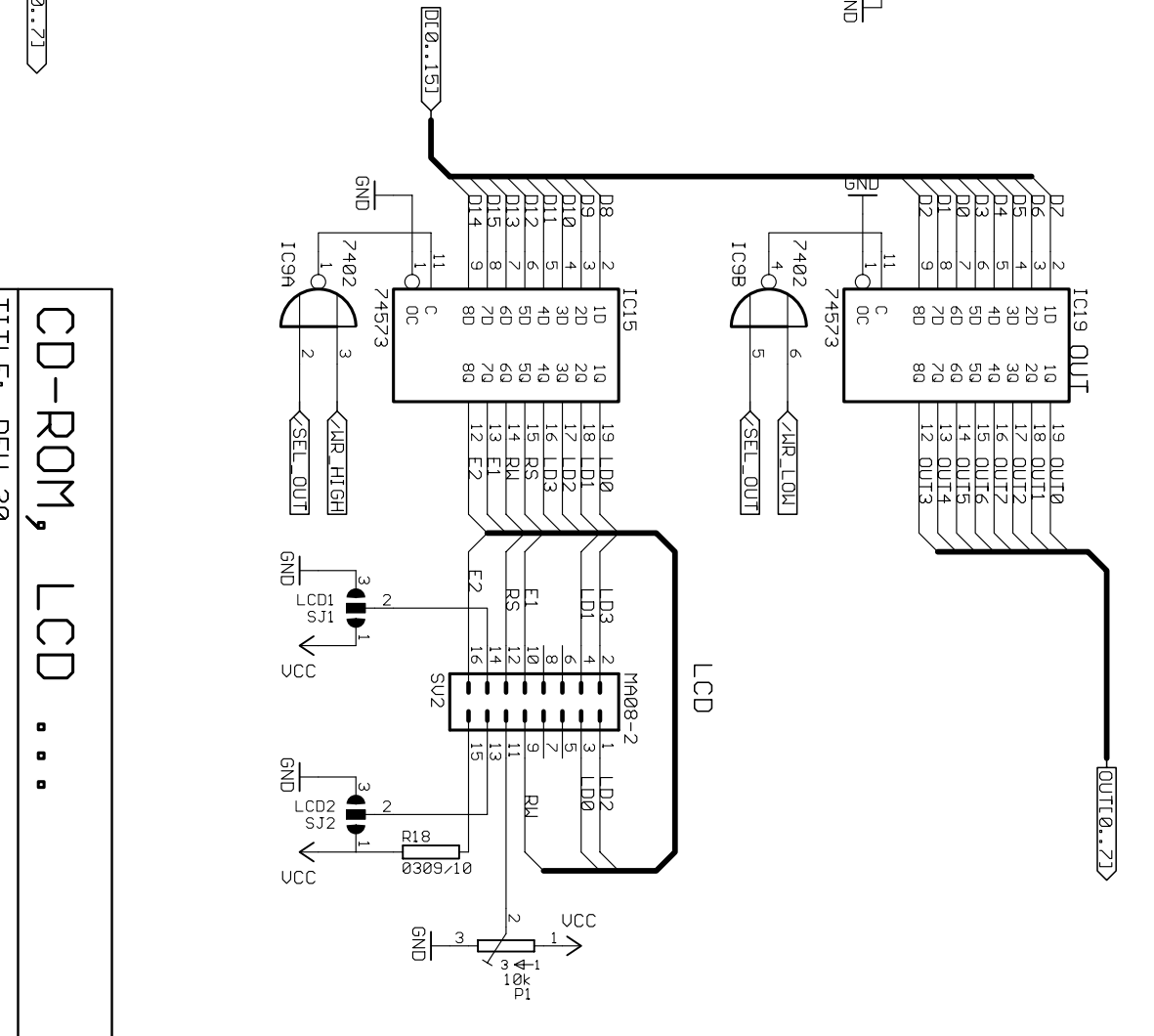
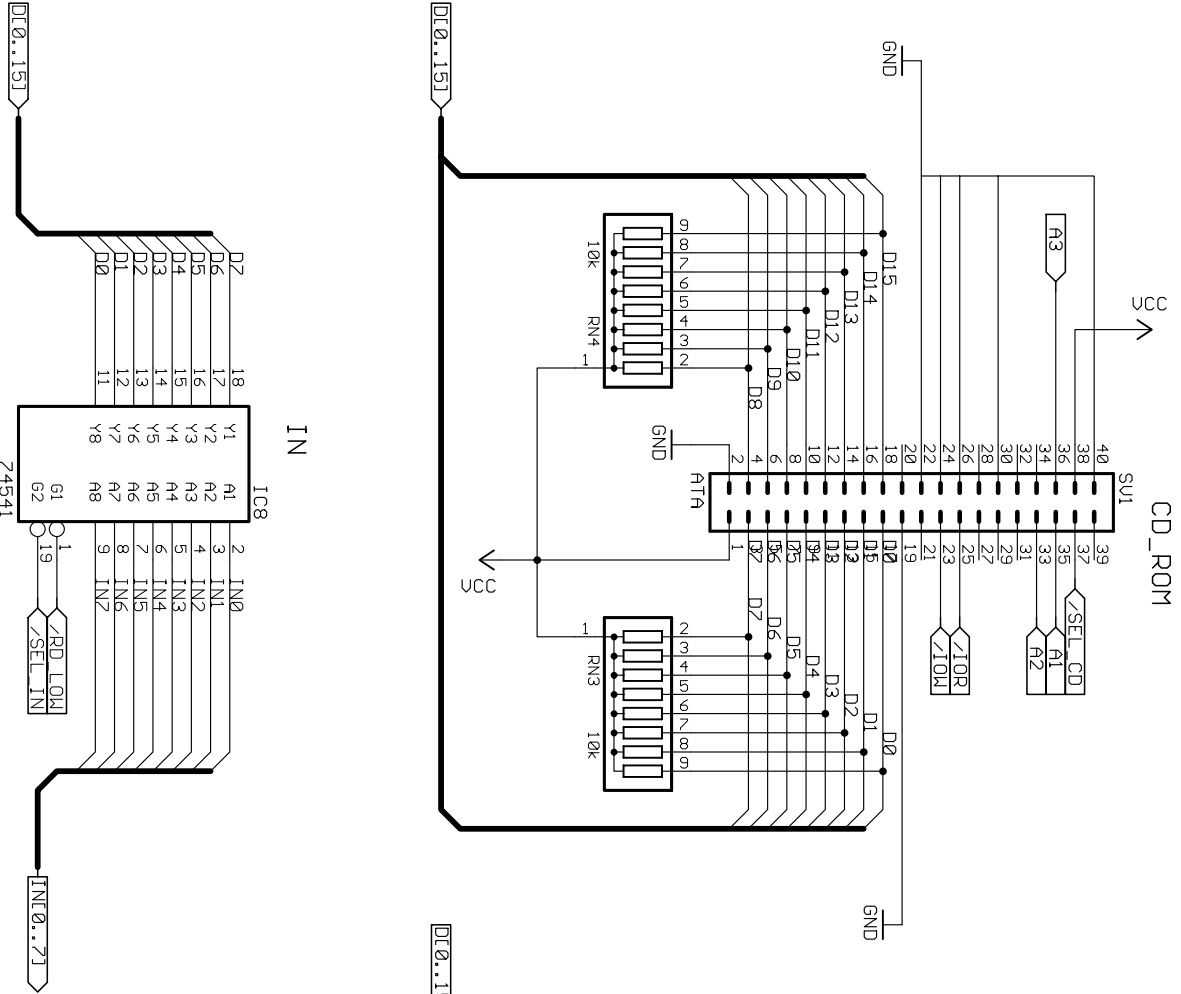
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Sheet: 1/1



CD-ROM, LCD

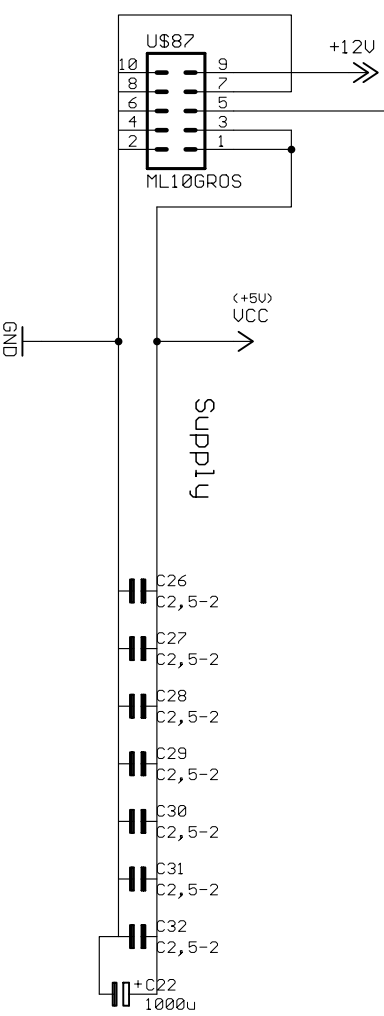
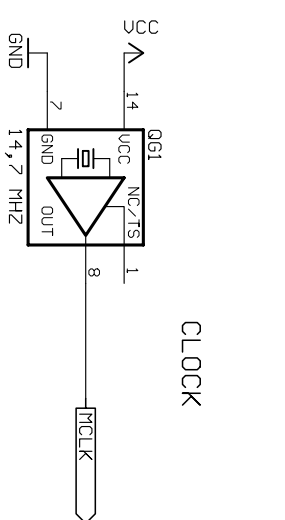
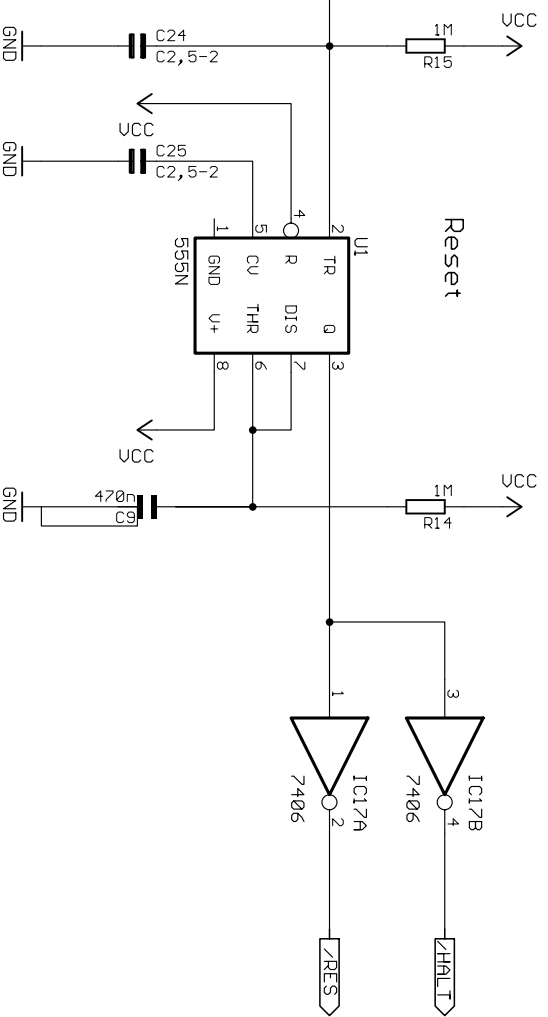
TITLE: REV 30

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Reset, CLK, EXP.

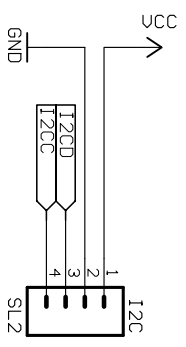
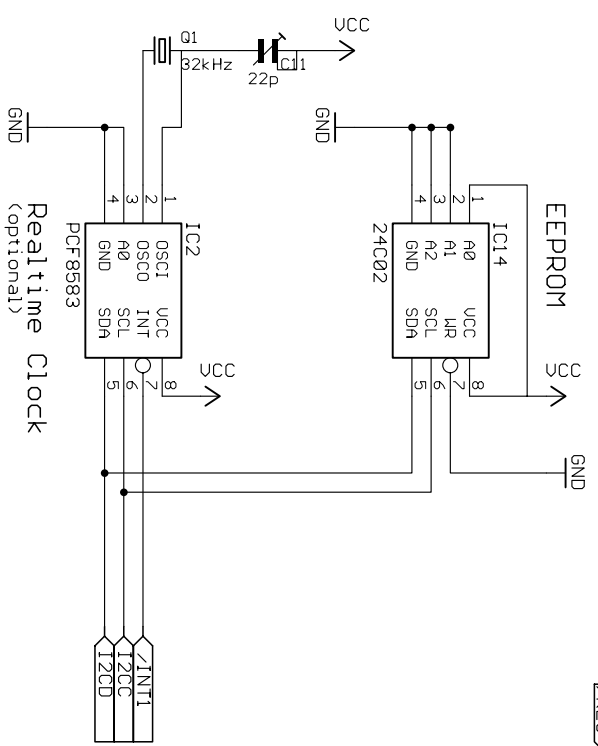
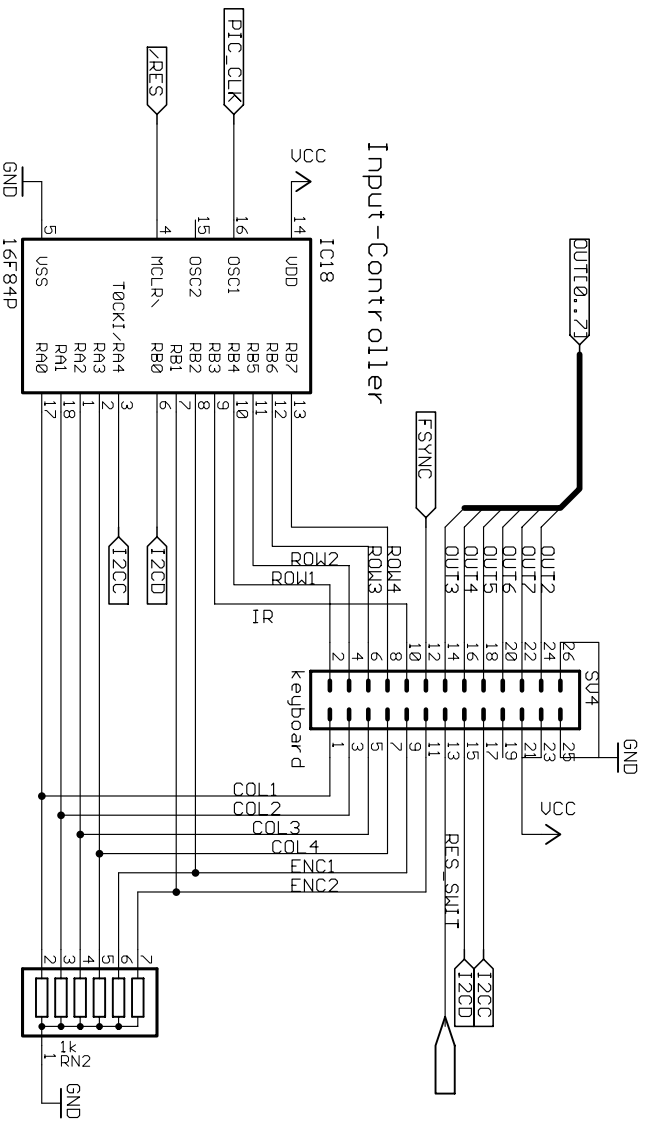
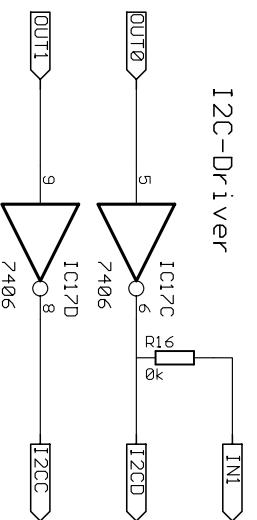
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I2C Bus

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